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Method and system for power control in radio transceivers

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Description

METHOD AND SYSTEM FOR POWER CONTROL IN RADIO TRANSCEIVERS

Field of the invention

The invention relates generally to power control in radio transmitters, and especially to transceivers used in telecommunications systems, such as used in mobile terminals.

Background of the invention

Because the number of users of mobile terminals has increased tremendously, there have been lots of efforts to increase the capacity of mobile networks. As one possible solution, the Code Division Multiple Access CDMA technology has been under discussion for years. In Europe, the UMTS research work has mostly concentrated on the wide band CDMA technology. On the other hand, there has also been a multitude of other research efforts relating to further development of the already existing Global System for Mobile communications GSM technologies. For example, Enhanced Data rates for GSM Evolution EDGE is currently coming to market.

In the GSM, the Gaussian Minimum Shift Keying GMSK modulation is used. On the contrary, in the EDGE, the 8PSK modulation scheme will be used. A remarkable difference between these two modulation schemes is that the 8PSK modulation is a non-constant envelope modulation scheme, whereas the GMSK is a constant envelope modulation scheme. This means that in the 8PSK modulation, some part of the information is contained in the amplitude of the envelope of the transmitted signal and some part is contained in the phase of the transmitted

signal. The amplitude modulation makes it more difficult to control the power of the transceiver. The main reason for the difficulty is that the varying amplitude causes variations in the peak signal power. The amplitude depends on the signals that are sent, and the peak power varies between time slots or data bursts that are sent with the same average output power.

Some solutions for controlling the power output of a radio frequency transmitter can be found in prior art. The European patent application 0 688 109 A2 describes an output power control arrangement for a burst transmitter. In '109 the idea is that the output power envelope shaping of the prior burst to be transmitted is controlled in a feedback loop producing a control signal. When the signal is to be transmitted using amplitude modulation, the feedback loop is switched off for the period of information transfer, but closed at other times, whereas for bursts to be transmitted with a constant envelope modulation the loop is not switched off.

International patent application WO 00/33477 presents a peak to average power ratio limiting apparatus to be used in a CDMA network. Because the air-interface bandwidth is shared between multiple users, the compound signals may have high peaks to average power ratio to be processed by the transceiver. Because compound signals are input to the power amplifier of a mobile terminal, the amplifier has usually a poor power efficiency. In '477 the system has a squared envelope magnitude predictor equivalent to a power estimation apparatus that estimates the squared magnitude of the modulated CDMA waveform envelope. The envelope is finally formed by the base band signal after quadruple modulation. The predicting requires excessive averaging in order to find

the average power through the burst, which results in a narrow resolution bandwidth.

A third prior art power output control system is presented in a published UK patent application GB 2 368 208 A. The system measures information relating to statistical variations in the amplitude of the information signal to be transmitted. The statistical variations are used to control a gain value of the radio frequency transmitter. The statistical amplitude variation of the non-constant envelope modulation is taken into account and compensated. This requires excessive computation as well.

It is an object of the invention to obtain a solution by means of which it is possible to bring about a system with which the output power of a radio transceiver can be controlled in a simple and reliable manner and the component count reduced by use of software control.

Summary of the invention

This and other objectives of the invention are accomplished in accordance with the principles of the present invention by providing a method or a system for controlling the power of the radio transceiver as described in the independent patent claims.

A power control system for a radio transceiver includes i) an amplifier for amplifying a signal to an amplified signal, the signal including data bursts, ii) means for obtaining a voltage corresponding to the power of the amplified signal, iii) a comparator for comparing said voltage with a reference voltage, adapted to produce a comparison result,

and iv) control means responsive to said comparator adapted to adjust a control signal of the amplifier if the comparing result shows that the voltage representing the power of the amplified signal deviates more than a predefined threshold value from the reference voltage. Further, the system includes time masking means adapted to measure the voltage, in at least one time window with a predefined length, of a first data burst to be used in the comparator. In the system, the control means are adapted to set the control signal of the amplifier after a predetermined time delay, after the time window has lapsed. The proposed system solves problems with power detection in EDGE and other non-constant envelope system.

A method for power control in a radio transceiver includes the steps of i) amplifying a signal to an amplified signal, the amplified signal including data bursts, ii) measuring a voltage, the voltage corresponding to the output power of the output signal, iii) comparing said voltage with a reference voltage, the comparison producing a comparison result, iv) in response to the comparing step, adjusting a control signal which is used in adjusting the amplifying step, if the result of the comparison step is that the voltage corresponding to the output power of the signal produced in the amplifying step deviates more than a predefined threshold value from the reference voltage, and v) selecting at least one time window with a predefined length for a data burst for measuring the voltage in the collecting step. The adjusting step is adapted to adjust the control signal after a predetermined time delay. The proposed method solves problems with power detection in EDGE and other non-constant envelope system.

Brief Description of the Drawings

In the following, the invention and its preferred embodiments are described more closely referring to the examples shown in FIG. 1-6 in the appended drawings, wherein:

FIG. **1** illustrates the power control circuit to be used for controlling the output power of the amplifier,

FIG. **2** illustrates a flow diagram showing the operation of the control means 124,

FIG. **3** is a flow diagram illustrating the operation of the system timer 116,

FIG. **4** shows a time mask used for an 8PSK modulation data burst,

FIG. **5A** shows the relation of subsequent bursts, the output signal values measured from them, and the timing of the control signals,

FIG. **5B** shows a table illustrating the data in the control means 124, and

FIG. **6** illustrates an embodiment of the invention implemented to be used in a microprocessor.

Like references refer to similar elements throughout the figures.

Detailed description of the invention

FIG. 4 shows a schematic presentation of a burst template of the EDGE 8PSK modulation. For the time axis, the figures under the axis correspond to the duration of each state of the burst in microseconds. When the burst is switched on at zero time, the transceiver power ramps up. The first and last 28 µs is for ramping up and down respectively. The actual sending of the payload data of the burst begins 28 µs after the beginning (T=0) of the burst, and has a duration of 542,8 µs. As specified in the specification 3GPP TS 45.005 V5.2.0 (Third Generation Partnership Project; Technical Specification Group; GSM/Edge Radio Access Network: Radio Transmission and Reception), for the envelope a specific time interval lasting altogether 4 µs is defined.

During the length ΔSWX1 of the time window SWX1 the modulation for both 8PSK and GMSK is essentially constant envelope modulation because of the tail symbols. Therefore, the position of sensing power does not need to be changed between different modulations. As already noted, getting an average value of the power during an EDGE burst would take too much processing power from the terminal equipment, or require different loop bandwidths, one for ramping and one for averaging the data part of the burst.

According to one aspect of the present invention a time window SWX1 is selected between to correspond the time interval from SWX1ON to SWX1OFF. Similarly, another time window SWX2 with length ΔSWX2 between SWX2ON and SWXOFF can be selected. These windows corresponds to the tail bits, the bits being sent in a constant envelope. The benefit of using

two windows is that if the output power is dropping through burst, a second window at the down ramp is necessary for detecting and compensating for it. Such dropping of the power during the burst can be anything from the power amplifier and after the amplifier 102.

The transmitted power level at these moments of time should, according to the specification TS 45.005 referred above, equal to 2.4 dB. The voltage V_{out} observed when the amplifier 102 is detected to transmit some signal S_{out} with a correct power level P_{out} is selected to present the reference voltage V_{ref}.

The 4 μs long sample comes from the ETSI 45.005 specification, which defines the 2+2 μs period before the modulation becomes evident. From the implementation point of view, it is beneficiary to sample at least 4 μs in order to get an average with a small enough statistical fluctuation. The length of the time window in which the measurement is made can be longer, e.g. it can be selected to correspond to the tail symbol duration, i.e. three symbols which have a duration of (48/13)*13 μs = 11 μs. This is the maximum time to get power measurement samples to average in software. In EDGE, as already noted, during the tail symbols there is only phase modulation but no amplitude modulation, which then enables the sample-measurements for a constant envelope.

FIG. 1 shows a schematic circuit controlling the output power of an amplifier 102. An input signal S_{in} with an initial power P_{in} is sent to the amplifier 102 which outputs a signal S_{out} with output power P_{out}. The reference power level $P_{out,\ meas}$ corresponding to the output power P_{out} is also obtained from

the amplifier 102. A voltage V_{out} corresponding to the reference power level $P_{out,\ meas}$ is detected and fed to a comparator 112. The comparator 112 compares the voltage V_{out} with a reference V_{ref} which represents the value of voltage V_{out} which should be detected when the amplification is performed correctly. The comparator 112 produces as ist output detected signal ΔV which is then led to an analog to digital converter ADC 118 which converts the detected signal ΔV into a digitised value $S\Delta V$.

The ADC 118 passes the digitised value $S\Delta V$ to a comparator 122. The comparator 122 compares the digitised value $S\Delta V$ with a predetermined threshold value. The comparator 122 passes the comparison result CR to control means 124.

The control means 124 read an old target power level $PL_{old\ target}$ from register 120. If the comparison result CR shows that the output voltage V_{out} deviates from the reference voltage V_{ref} more than a predefined threshold value, i.e. that the norm calculated for the digitised value $S\Delta V$ is larger than the predefined threshold value, the control means 124 control the amplifier 102 by adjusting the value of a control signal $V_{control}$. The control means 124 also write a new target power level value $PL_{new\ target}$ into the register 120.

Main timer 114 provides a signal RS that is used in the control means 124 and in a counter 116 for timing purposes. The counter 116 changes the position of the switch SW1 by sending a control signal CS according to instructions SW it has obtained from the control means 124. The switch SW1 switches between the amplifier output T1 and terminal T2, and connects the amplifier output T1 or the terminal T2 to the

terminal T3. The terminal T2 may be grounded; hence the value of the detected signal ΔV can be easily estimated.

The system may be implemented using computer software in such a way that the sampling performed by the ADC 118 is triggered in terms of bits in a burst the transmission of which is to be controlled, and then timed by a clock used for the microprocessor wherein the computer code is executed. The timing may be based on GSM timer unit in base band, for example, if the amplifier is a GSM amplifier.

Figure 2 illustrates the operation of the control means 124 in more detail. If the system is implemented using a software code which is executed in a microprocessor, then this is preferably performed as a process in the microprocessor. In step G1, a time window i.e. monitoring window is defined. Within this time window the ADC 118 samples the detector signal.

The position of the switch SW1 may be changed by the counter 116. Further, a time delay TD relating to the system can be set up and burst timing defined. After defining the time windows, the number of clock cycles corresponding to the duration or moment of each operation is calculated in step G3. For a software implementation, the positions of time windows SWX1, SWX2, ... are chosen and defined in bits or steps with reference to the system timer.

In step G5, the instructions about the time windows SWX1, SWX2, ... are stored into register 120, and, correspondingly, in step G7 the instructions about the time windows SWX1, SWX2, ... are stored into the system timer 116 which may be a local oscillator or use the main timer 114 for timing

purposes. The system timer 116 may also be a counter implemented by computer software. The steps G1 to G7 are performed before the control means 124 start controlling the amplifier 102, e.g. in the manufacturing or design stage of a mobile terminal. Different instructions can be computed and stored when deemed necessary, such as if the timing changes, for example, which might be the case of a multi-band terminal.

In step G9, the control means 124 receive the control signal CR from the comparator 122 which can correspond to a routine run in the software, for example. In step G11 the control means 124 check whether there is a need to adjust the power level.

If the result of the comparison shows that the power level value PL has to be adjusted, the power level value PL is computed in step G13, and in step G14 it is stored into the register 120 as the new target power level $PL_{new\ target}$. After storing the power level value PL in step G14, the control signal $V_{control}$ is adjusted in step G16 corresponding to the power level value PL when needed, i.e. when a burst using the same power is commanded.

If the result of the comparison in step G11 shows that there is no need to adjust the power level PL, the control signal $V_{control}$ is adjusted in step G16 just in order to ensure that the control signal $V_{control}$ value is appropriate. In this case, after adjusting or checking the control signal $V_{control}$ value in step G16, the control returns to step G9 for obtaining new comparison results CR.

FIG. 3 illustrates the operation of the timing process in system timer 116. In step H1, the control signal CS is set to trigger the ADC to sample voltage V_{out}. In step H5, a counter variable is reset. Then the system timer 116 receives a signal RS from the main timer 114 which may correspond e.g. to a local oscillator. The counter variable is increased in step edge H9 corresponding to the signal RS detected in step H7. In step H11, it is examined whether the counter parameter is between the values presenting moments in time SWX1ON and SWX1OFF for opening and closing the time window SWX1, or SWX2ON and SWX2OFF for opening and closing the time window SWX2, respectively, which have already been determined in step G3.

If the counter parameter is between values SWX1ON and SWX1OFF i.e. within the time window SWX1 the control is passed to the step H15 where the control signal CS is modified so that the switch SW1 connects the comparator 112 output T1 and T3. Then the control returns to the step H7, i.e. a next signal RS is counted. Similarly is performed, if the counter parameter lies in the time window SWX2, i.e. between SWX2ON and SWX2OFF.

If the counter parameter does not fall between any of these two parameter pair values, then in step H13 the control signal CS is checked and adjusted if necessary to ensure that the switch SW1 connects the terminals T2 and T3. After this the control is returned to step H7 for collecting a new signal RS.

FIG. 5A illustrates subsequent data bursts BA, BB, BC and BD. The envelope of each of data bursts BA to BD is similar to

the envelope of the data burst presented in FIG. 4. In the first data burst BA there are two time windows SWA1, SWA2 used for selecting a part of the reference power level $P_{out, meas}$ to obtain the detected signal ΔV in the first data burst BA. The digitised value SΔV of the detected signal ΔV is used in the comparator 122 when comparing the digitised value SΔV against a predetermined threshold value.

In FIG. 5A there are only four data bursts BA to BD presented, but, in principle, the data bursts extend all over the transmission period. In the figure, TCA, TCB, TCC and TCD illustrate moments in time at which the control means 124 are ready with the comparing step G11 and the steps G13 and G14 are being completed. This is usually a bit later than any of the corresponding time windows (SWA1, SWA2 for TCA; SWB1, SWB2 for TCB; SWC1, SWC2 for TCC; and SWD1, SWD2 for TCD), because the processing of the information by the comparator 112, ADC 118, comparator 122, and control means 124 requires some time.

Time delay TD shows the delay between the beginning (TIB, TIC, TID) of the subsequent data burst (BB, BC, BD) and the moment in time (TCA, TCB, TCC) at which a control signal $V_{control}$ for the previous burst (BA, BB, BC, respectively) has been determined. It also illustrates that in step G16 the adjustment of the control signal $V_{control}$ must be delayed in the control means 124. The delaying has to be done because the amplitude of an 8PSK modulated burst may not be altered within the burst because this might corrupt some data contained in the amplitude, for example. Hence the new control signal $V_{control}$ obtained at moment in time TCA must be used at a later point in time, i.e. at the beginning of a

subsequent burst (BB, BC, BD) the controlling point in time being then TIB, TIC or TID, correspondingly. Preferably, in order to avoid sending a large number of data bursts BB, BC, BD each being broadcast with a wrong power level, the subsequent burst before the beginning of which the correction to the amplifier 102 is sent is the next data burst BB.

FIG. 5B is a table showing some measurement values for the voltage V_{out} during sequential data bursts at time windows SWX1 and SWX2 corresponding to time windows SWA1, SWA2, SWB1, SWB2, and so forth. For X = A, the average value during the time window SWA1 of the voltage V_{out} is 0.25 V, whereas the reference voltage V_{ref} = 0.24 V. In the second time window SWA2 the voltage V_{out} = 0.26 V. The computed average of the different voltages V_{out} differs from the reference voltage V_{ref} 0.015 V. This corresponds to a 6.3% excess with respect to the reference voltage V_{ref}. If the initial value of the control signal $V_{control}$ passed to the amplifier 102 were for this burst 5 V, it would have to be decreased by 6.3%, the new value being 4,67 V. The control signal $V_{control}$ is changed in step G16 in the control means 124.

For the next data burst BB (for which X=B) during the time mask SWB1 the voltage V_{out} 0.24 V is measured, and for SWB2, the voltage V_{out} of 0.25 V is measured. The reference voltage V_{ref} is again constant 0.24 V, and the average calculated from both voltages V_{out} measured at time windows SWB1 and SWBV2 values differs 5 mV from the reference voltage V_{ref}. The old power level value $PL_{control,\ old}$ equals for this burst 4.67 volts and the new power level value $PL_{control,\ new}$ has to be given a value of 2,1 % less for the next data burst. Control signal $V_{control}$ is again changed after the time delay TD lapses, i.e. the control means 124 have a delay between the obtaining the

new control signal $V_{control}$ for the next burst BC, and the actual changing of the control signal $V_{control}$ in the amplifier 102 which takes place at the beginning of the subsequent data burst TIC. This on its behalf causes a corresponding change for the output power P_{out} of the data burst BC and so forth.

Figure 6 illustrates an embodiment of the invention implemented to be used in a microprocessor, for example with the help of a software code. The amplifier 102 receives a signal S_{in} with initial power P_{in} and amplifies it to an output signal S_{out} having an output power P_{out}. A reference power level $P_{out,\ meas}$ presenting the output power P_{out} of the signal S_{out} is collected using a sensor, such as a coupler, and fed to a detector 601. The detector 601 outputs a detector voltage V_{det} being responsive to the reference power level P_{out}. The detector voltage V_{det} is passed to the processing block 603 which comprises ADC means 118, processor/system timer 605 and a digital-to-analog converter DAC 607.

The processor/system timer 605 trigger the ADC 118, and digitised values of V_{det} are read to the analysing means in the processor/system timer 605. The processor/system timer 605 analyses and controls the control voltage $V_{control}$. The controlling is performed so that the processor/system timer 605 sends a control signal to the DAC 607 which then passes the analog control voltage $V_{control}$ to the amplifier 102.

More precisely, all tasks as described with reference to Figure 1 can be implemented also using computer software. According to one embodiment of the invention, such an implementation follows the guidelines discussed with reference to Figure 6. Then the system includes an amplifier

for amplifying signal including data bursts. A sampled signal corresponding the amplified signal is compared with a reference value. If the result of the comparison shows that the signal presenting the amplified signal differs more than a predefined threshold value from the reference value, a control signal of the amplifier is adjusted by control means of the system.

The signal corresponding to the amplified signal is selected by a time window from a first data burst, and the control means are adapted to adjust the control signal of the amplifier, to have an effect from the beginning of a subsequent data burst. This is particularly useful when the data bursts in question include also amplitude modulation part, because it saves a great deal of processing in getting an average value of the power.

In accordance with one aspect of the present invention, the signal is during at least one time window located at an edge of the active burst. Preferably, this may be a ramp up or a ramp down position of the active burst. The top of up- and down ramping periods in both 8PSK and GMSK, because of the tail symbols, has a constant envelope, i.e. no amplitude modulation.

In accordance with another aspect of the present invention, the predetermined time delay corresponds to the time between obtaining the sample of the signal and the time at which the subsequent burst may begin. Preferably, said subsequent burst is the next burst to the burst for which the part of the signal was selected. In this way the timing of the correction does not interfere with the possible amplitude modulation

present in the burst being sent, i.e. that the correction is done for a whole burst, not for only a part of it.

The invention can be utilised not only in mobile terminals, but also in any devices that include a transceiver transmitting a signal containing data bursts. Such a device may be a base station used in mobile networks, for example.

Although the invention was described above with reference to the examples shown in the appended drawings, it is obvious that the invention is not limited to these, but it may be modified by those skilled in the art without departing from the scope and the spirit of the invention.

For example, the number and length of time windows may be different from two and 4µs, and the delaying the amplifier 102 control may take place in the ADC 118, in the comparator 122, or in the amplifier 102 instead of taking place in the control means 124. Eventually the comparator can be an operational amplifier and a switch controlled by a timer can sample voltage V_{out}.

List of symbols and references used

102	amplifier
112	comparator
114	main timer
116	system timer
118	analog-to-digital converter ADC
120	register
122	comparator
124	control means
601	detector
603	processing block
605	processor/system timer
607	digital-to-analog converter DAC

ΔV	detected signal
SΔV	digitised value of **ΔV**
Pout	output power
Vout	voltage
Pout, meas	reference power level
Pin	initial power
Sin	input signal
Sout	output signal
PLold target	old target power level
PLnew target	new target power level
RS	signal used for timing
CS	control signal
Vcontrol	control signal
Vdet	detector voltage
Vref	reference voltage

SWX1, SWX2	time windows
SWX1ON, SWX2ON	moment in time for opening the time window **SWX1, SWX2**
SWX1OFF, SWX2OFF	moment in time for closing the time window **SWX1, SWX2**
ΔSWX1, ΔSWX2	length of time window **SWX1, SWX2**
TCA, TCB, TCC, TCD	moments in time
BA, BB, BC, BD	data bursts

Claims

1. A power control system for a radio transceiver, the system including:
- an amplifier (102) for amplifying a signal (Sin) to an amplified signal (Sout), the signal (Sout) including data bursts (BA, BB, BC, BD);
- means (102) for obtaining a voltage (Vout) corresponding the power (Pout) of the amplified signal (Sout);
- a comparator (112) for comparing said voltage (Vout) with a reference voltage (Vref), adapted to produce a comparison result (CR);
- control means (124) responsive to said comparator (122) adapted to adjust a control signal (Vcontrol) of the amplifier (102) if the comparing result (CR) shows that the voltage (Vout) presenting the power (Pout) of the amplified signal (Sout) deviates more than a predefined threshold value from the reference voltage (Vref);
characterised in that:
the system further includes:
- time masking means (114, 116, SW1) adapted to measure the voltage (Vout), in at least one time window (SWA1, SWA2) with a predefined length (ΔSWA1, ΔSWA2), of a first data burst (BA) to be used in the comparator (122); and wherein:
- the control means (124) are adapted to set the control signal (Vcontrol) of the amplifier (102) after a predetermined time delay (TD), after the time window (SWA1, SWA2) has lapsed.

2. A system according to claim 1,
wherein: the time masking means (114, 116, SW1) are

adapted to select the time window (SWA1, SWA2) located at an edge (SW1AON, SW1AOFF; SWA2ON, SWA2OFF) of an active burst (BA).

3. A system according to claim 2, **wherein:** said edge is in a ramp up or a ramp down position of the first active burst (BA).

4. A system according to claim 1, **wherein:** the predetermined time delay (TD) corresponds to the delay between the moment in time (TCA) at which the control signal value (Vcontrol) is obtained, and the time (TIB, TIC, TID) at which a subsequent burst (BB, BC, BD) begins.

5. A system according to claim 4, **wherein:** said subsequent burst is the next burst (BB) to the burst (BA) for which the voltage (Vout) is measured.

6. A system according to claim 1-5, **wherein:** the predefined length (ΔSWA1, ΔSWA2) of at least one of the timing windows (SWA1, SWA2) is approximately 4 microseconds.

7. A system according to any one of claims 1-6, **wherein:** the length (ΔSWA1, ΔSWA2) of at least one of the timing windows (SWA1, SWA2) is variable.

8. A system according to any one of claims 1-7, **wherein:** the time masking means (114, 116, SW1) and/or control means (124) are at least partially implemented using software code that is run in a processor.

9. A mobile terminal
characterised in that:
in the mobile terminal a power control system according to any one of the preceding claims 1-8 is used.

10. A base station terminal
characterised in that:
in the base station a power control system according to any one of the preceding claims 1-8 is used.

11. A base station terminal
characterised in that:
in the base station a power control system according to any one of the preceding claims 1-8 is used.

12. A method for power control in a radio transceiver, the method including the steps of:
- amplifying a signal (Sin) to an amplified signal (Sout), the amplified signal (Sout) including data bursts (BA, BB, BC, BD);
- measuring a voltage (Vout), the voltage (Vout) corresponding to the output power (Pout) of the output signal (Sout);
- comparing said voltage (Vout) with a reference voltage (Vref), the comparison producing a comparison result (CR);
- in response to the comparing step, adjusting a control signal (Vcontrol) which is used in adjusting the amplifying step, if the result (CR) of the comparison step is that the voltage (Vout) corresponding to the output power (Pout) of the signal (Sout) produced in the amplifying step deviates more than a predefined threshold value from the reference voltage (Vref);

characterised in that:
the method further includes the step of:
- selecting at least one time window (SWA1, SWA2) with a predefined length (ΔSWA1, ΔSWA2) for a data burst (BA) for measuring the voltage (Vout) in the collecting step; and wherein:
- the adjusting step is adapted to adjust the control signal (Vcontrol) after a predetermined time delay (TD).

13. A method according to claim 11,
wherein: the selecting step is adapted to measure a voltage (Vout) of the data burst (BA) located at an edge (SW1AON, SW1AOFF; SWA2ON, SWA2OFF) of the data burst (BA).

14. A method according to claim 12,
wherein: said edge is in a ramp up or a ramp down position of the data burst (BA).

15. A method according to claim 11,
wherein: the predetermined time delay (TD) corresponds to a time (TCA) between determining a control signal (Vcontrol) and the time (TIB, TIC, TID) at which a subsequent burst (BB, BC, BD) begins.

16. A method according to claim 14,
wherein: said subsequent burst is the next burst (BB) to the burst (BA) during which the voltage (Vout) was measured.

17. A method according to any one of claims 11-15,
wherein: the predefined length (ΔSWA1, ΔSWA2) of at least

one of the timing windows (SWA1, SWA2) is approximately 4 microseconds.

18. A method according to any one of claims 11-16, **wherein:** the length (ΔSWA1, ΔSWA2) of at least one of the timing windows (SWA1, SWA2) is variable.

19. A method according to any one of claims 10-17, **wherein:** the comparison and/or controlling step are at least partially implemented using software code.

20. A mobile terminal **characterised in that:** in the mobile terminal a power control method according to any one of the preceding claims 10-17 is used.

21. A base station terminal **characterised in that:** in the base station a power control method according to any one of the preceding claims 10-17 is used.

Abstract

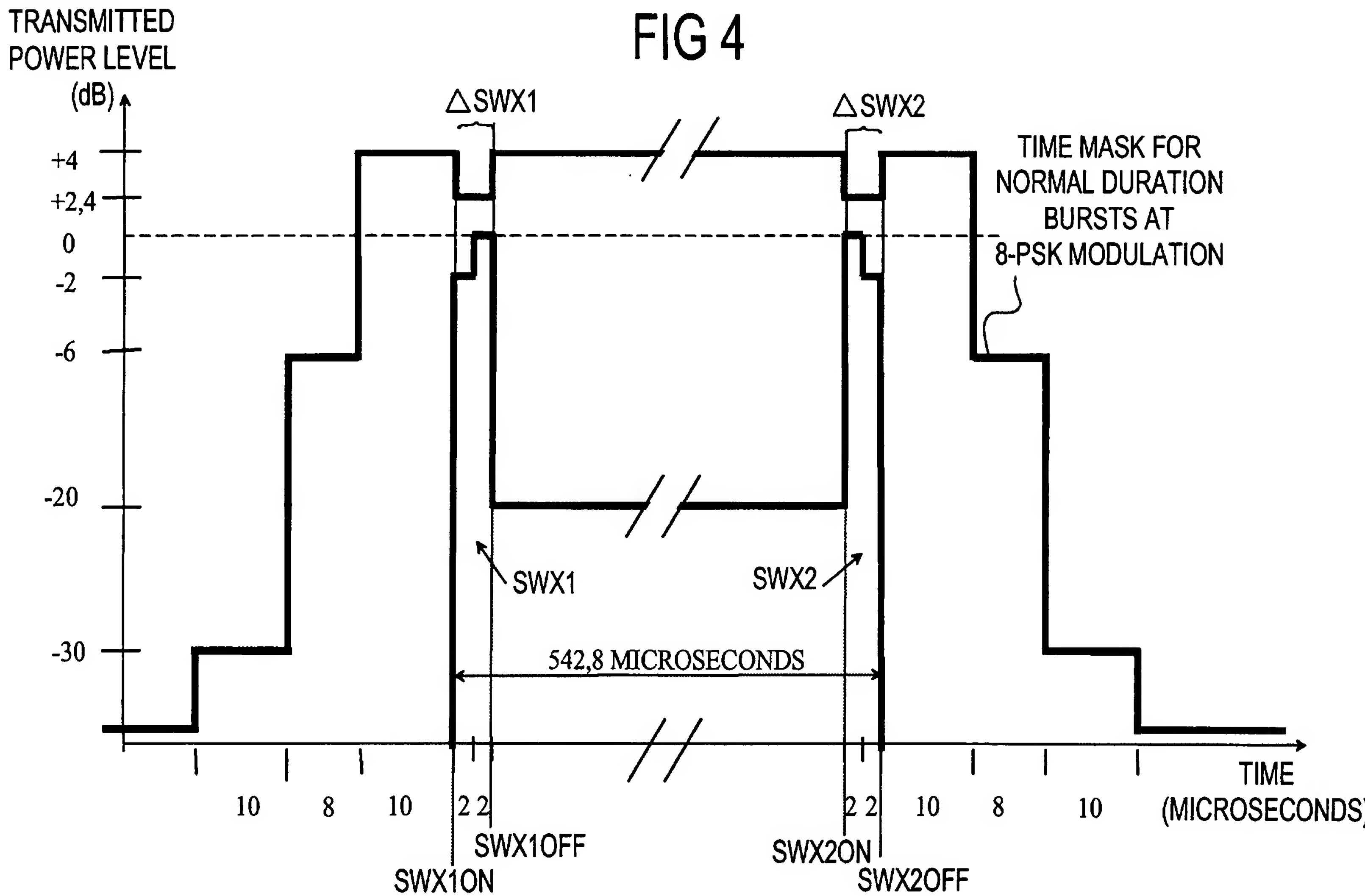
METHOD AND SYSTEM FOR POWER CONTROL IN RADIO TRANSCEIVERS

An amplifier amplifies signal including data bursts. A signal corresponding the amplified signal is compared with a reference value and if the result of the comparison shows that the signal presenting the amplified signal differs more than a predefined threshold value from the reference value, a control signal of the amplifier is adjusted by control means of the system.

The signal corresponding to the amplified signal is selected by a time window from a first data burst, and the control means are adapted to adjust the control signal of the amplifier after a predetermined delay, to have an effect from the beginning of a subsequent data burst. This is particularly useful when the data bursts in question include also amplitude modulation part, because it saves a great deal of processing in getting an average value of the power.

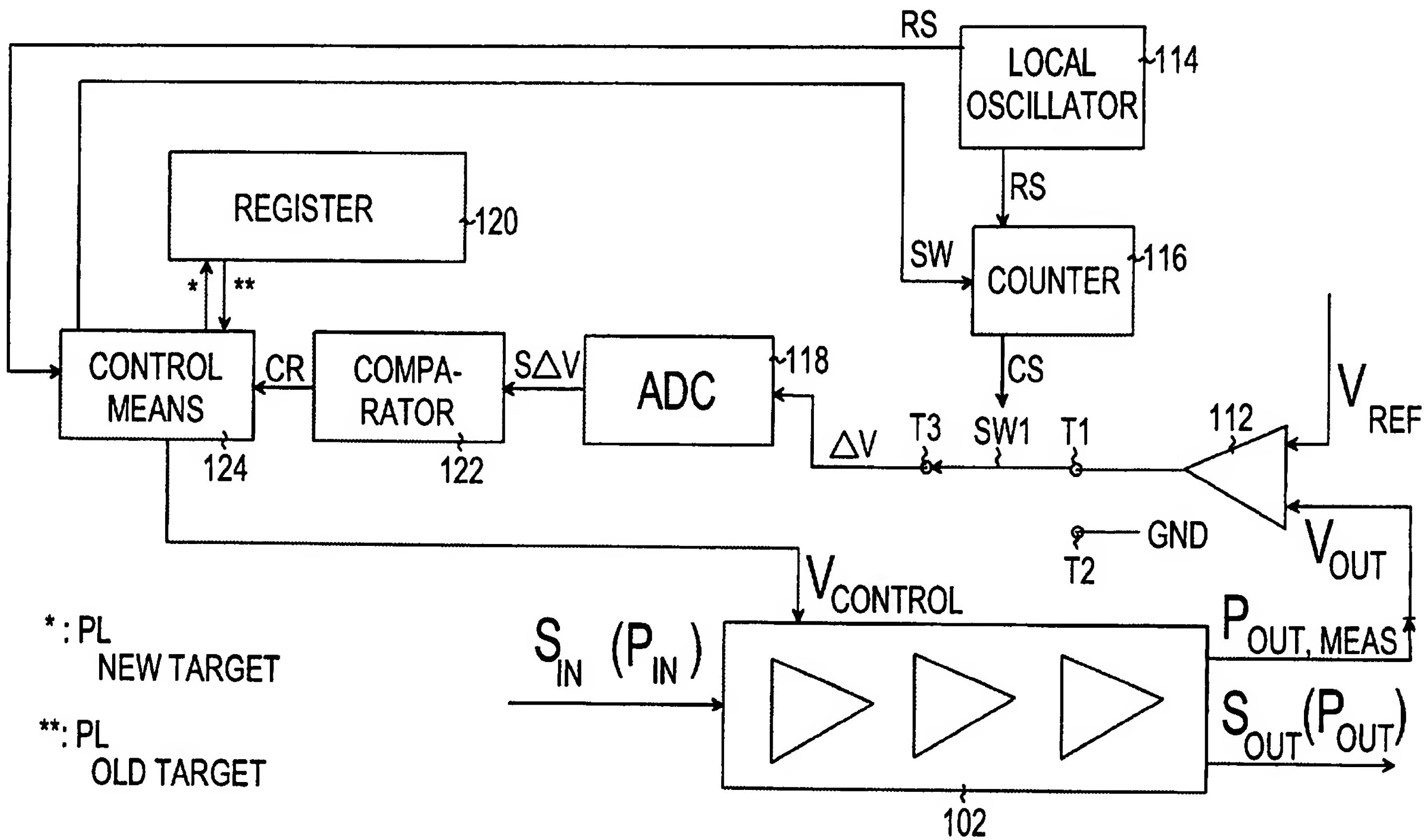
Figure 4

FIG 4



TRANSMITTED POWER LEVEL (dB)
+4
+2,4
0
-2
-6
-20
-30
ΔSWX1
ΔSWX2
TIME MASK FOR NORMAL DURATION BURSTS AT 8-PSK MODULATION
SWX1
SWX2
542,8 MICROSECONDS
10
8
10
2 2
2 2
10
8
10
TIME (MICROSECONDS)
SWX1OFF
SWX1ON
SWX2ON
SWX2OFF

FIG 1



LOCAL OSCILLATOR
114
RS
RS
COUNTER
116
SW
CS
REGISTER
120
*
**
CONTROL MEANS
124
CR
COMPA-RATOR
122
SΔV
ADC
118
ΔV
T3
SW1
T1
T2
GND
112
V REF
V OUT
V CONTROL
S IN (P IN)
P OUT, MEAS
S OUT (P OUT)
102
*: PL NEW TARGET
**: PL OLD TARGET

FIG 2

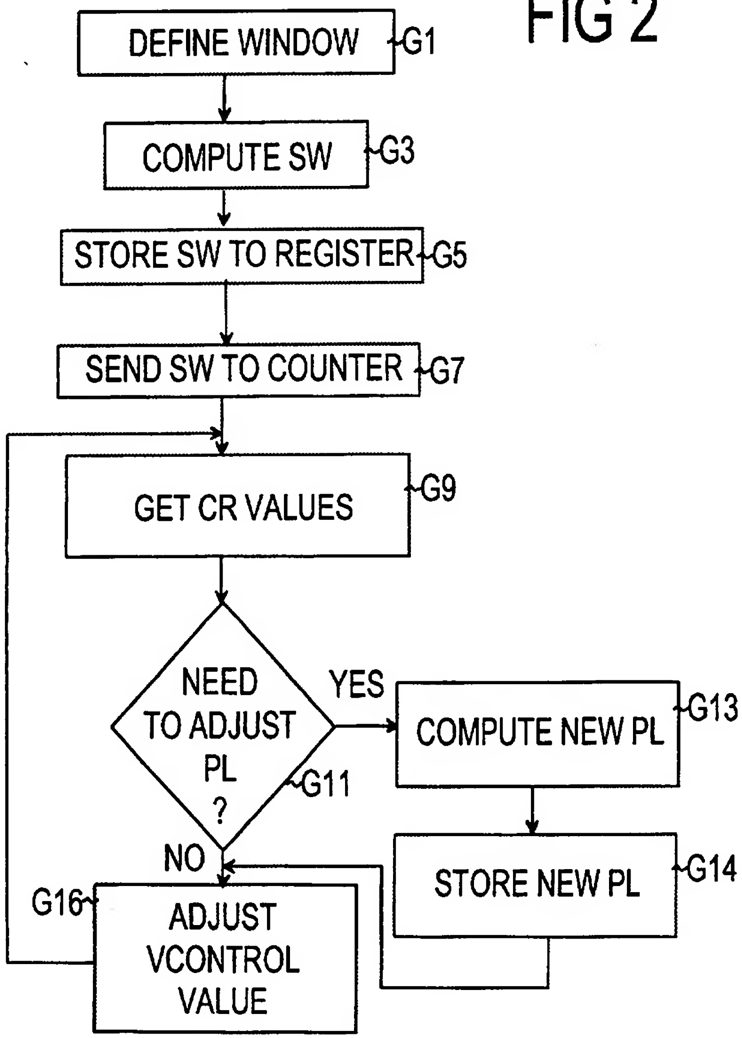

DEFINE WINDOW
G1
COMPUTE SW
G3
STORE SW TO REGISTER
G5
SEND SW TO COUNTER
G7
GET CR VALUES
G9
NEED TO ADJUST PL ?
G11
YES
NO
COMPUTE NEW PL
G13
STORE NEW PL
G14
ADJUST VCONTROL VALUE
G16

FIG 3

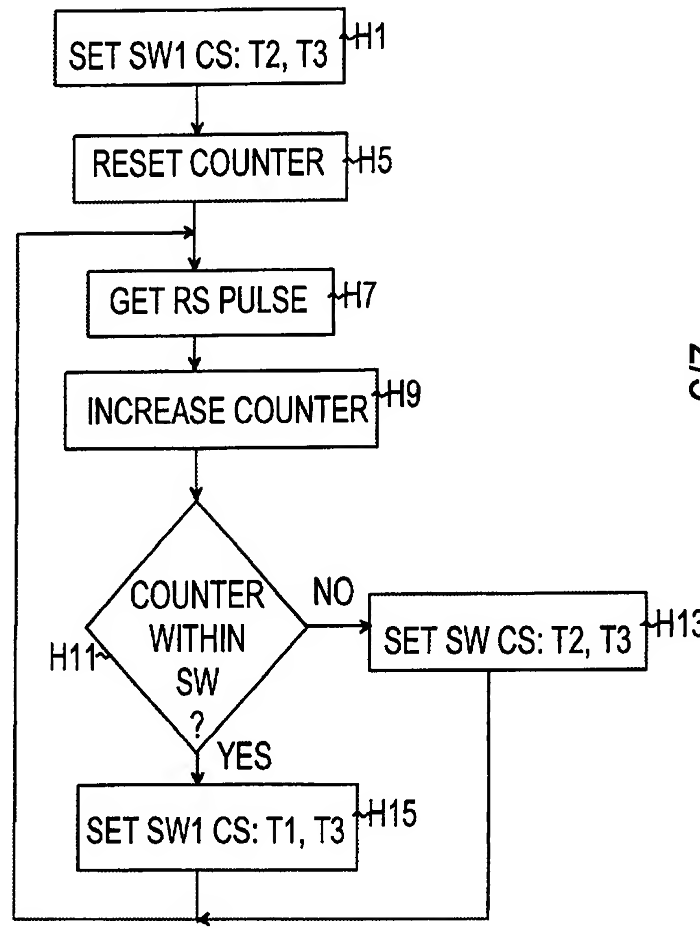

SET SW1 CS: T2, T3
H1
RESET COUNTER
H5
GET RS PULSE
H7
INCREASE COUNTER
H9
COUNTER WITHIN SW ?
H11
NO
YES
SET SW CS: T2, T3
H13
SET SW1 CS: T1, T3
H15

FIG 4

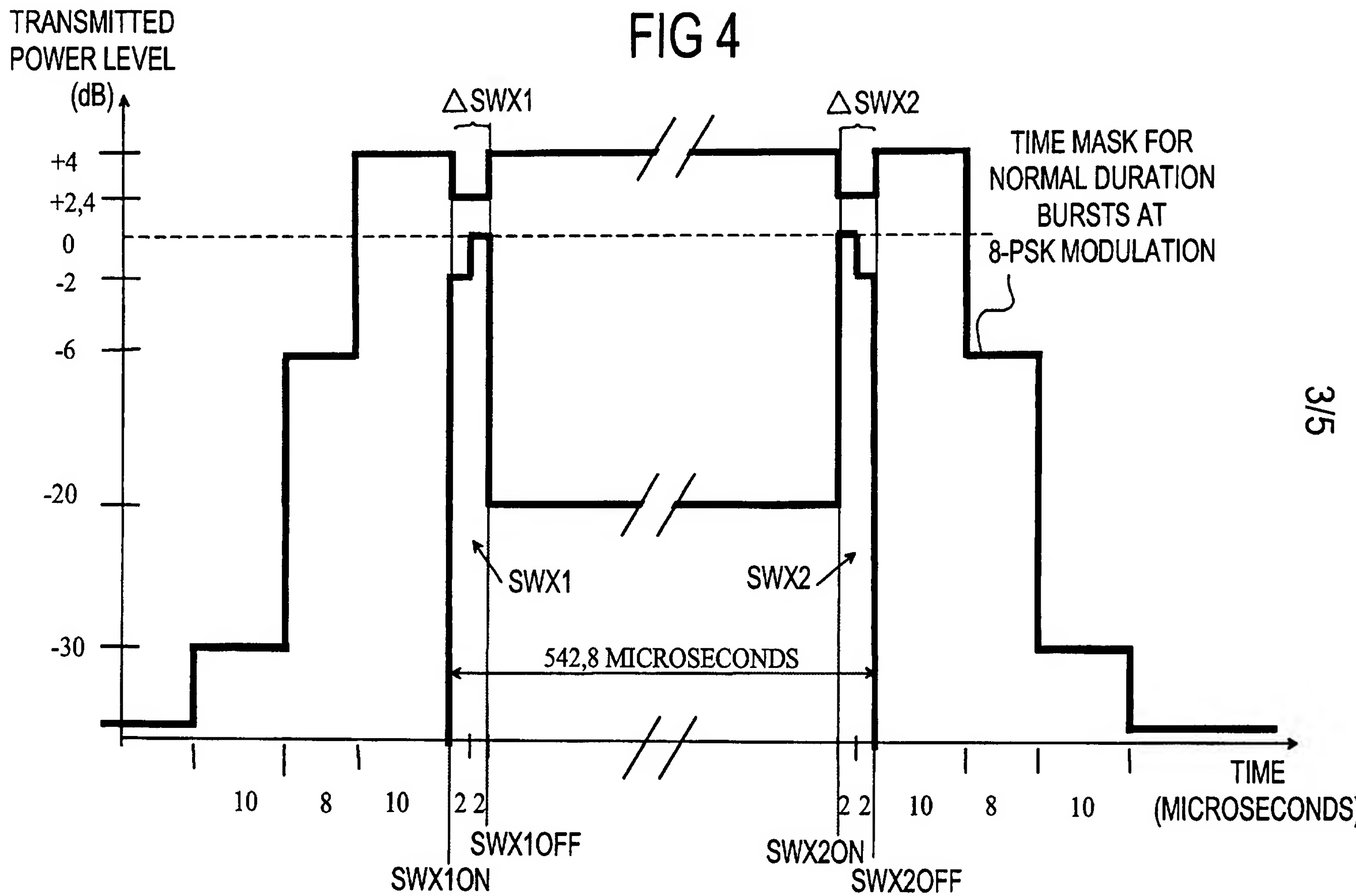
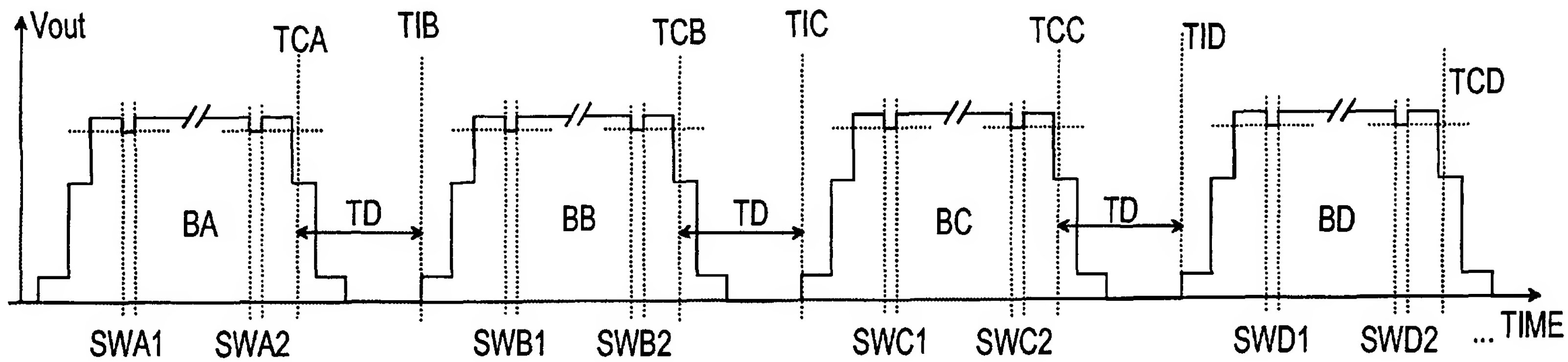

TRANSMITTED POWER LEVEL (dB)
+4
+2,4
0
-2
-6
-20
-30
ΔSWX1
ΔSWX2
TIME MASK FOR NORMAL DURATION BURSTS AT 8-PSK MODULATION
SWX1
SWX2
542,8 MICROSECONDS
10
8
10
2 2
2 2
10
8
10
TIME (MICROSECONDS)
SWX1OFF
SWX1ON
SWX2ON
SWX2OFF

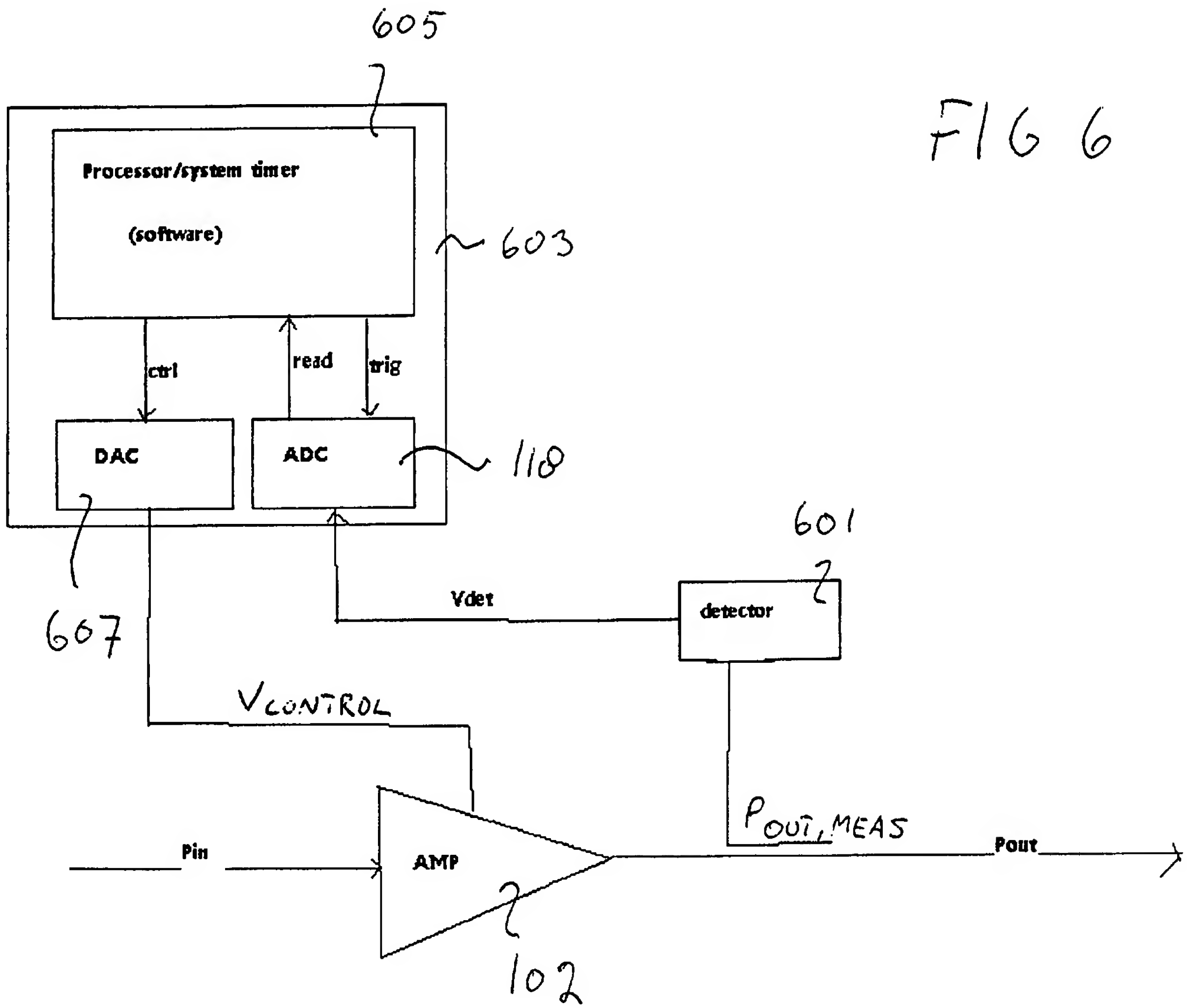
FIG 5A



X	Vout (SWX1)	Vout(SWX2)	Vref	ΔVout	Vcontrol	Vcontrol CHANGE FOR NEXT X ΔVcontrol/Vcontrol
A	0,25	0,26	0,24	0,015	5,00	-6,3 %
B	0,24	0,25	0,24	0,005	4,67	-2,1 %
...	...	...				

FIG 5B

FIG 6


605
Processor/system timer
(software)
603
ctrl
read
trig
DAC
ADC
118
607
601
Vdet
detector
$V_{CONTROL}$
$P_{OUT,MEAS}$
Pin
AMP
Pout
102